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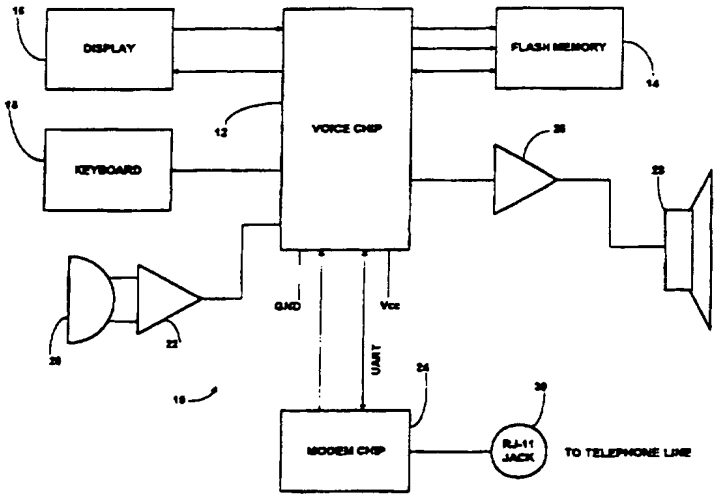

(57) Abstract

A portable device is disclosed which permits the user to record, edit, play and review voice messages and other audio material which may be received from, and subsequently transmitted to, a remote voice processing or interactive voice response (IVR) host computer over a communication link. A preferred device contains its own power source, integrated circuitry and control buttons to permit the localized recording, editing, storage and playback of audio signals through a built-in speaker (28), microphone (20), and removable memory card (14). The device also contains a standard RJ-11 telephone jack (30), modem chip set (24), and DTMF tone decoder to permit the transmission and control of audio signals to and from a host computer. The device contains circuitry which permits it to transmit and receive audio signals at a rate substantially faster than originally recorded.

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PERSONAL AUDIO MESSAGE PROCESSOR AND METHOD

Field of the Invention

The present invention relates generally to dictation devices and more particularly, concerns a method and portable apparatus for audio communication, including the recording and editing of voice mail and its transmission and reception over common electrical communication media or data links.

Background of the Invention

All electronic message systems, with the exception of voice-mail, have intermediate devices or storage media whereby data may be transferred, preferably at a high transmission rate, over a standard communication link and stored in a storage medium or onto an unattended device for later off-line access, review and editing by the intended user.

In the case of a facsimile transmission, an image is scanned by the transmitter and then transmitted and ultimately printed at a remote site for off-line utilization by the intended receiver. In the case of electronic mail, data is generated on a computer and then transmitted and stored either directly on the intended user's unattended computer or on a central host computer for subsequent retrieval by the intended user. When the intended user accesses his computer, either the E-mail is already resident or he finds a message indicating that he has mail and explaining how he can retrieve it. Once the E-mail is retrieved, it likewise may be read, reviewed and manipulated by the intended user off-line.

Similarly, utilities exist for both facsimile and E-mail messages whereby messages may be selected from a host by an authorized user for subsequent transmission to the user's E-mail address or unattended facsimile machine.

For both E-mail and facsimile, the use of a telephone link is limited to the transmission of the data and the transmission of control codes for that data.

In sharp contrast, voice messages and voice-text are currently recorded by the sender and retrieved by the intended recipient only in real-time. A voice mail user is limited to using a telephone handset or speaker-phone to record and listen to voice messages directly. There exist no devices to store voice messages and likewise there exists no method or utility to scan and select personal voice messages or public announcements from a host for subsequent high speed transmission to a device for subsequent off-line review by the user.

Voice messaging, limited to on-line and real-time transmission and physically requiring access to a telephone set is unfortunate, particularly because voice communication inherently does not require any external hardware or instrumentation other than a mouth and an ear for a human being to create or access it. Speech is the most natural and sufficient form of communication. Speech is hands-free requiring neither writing instrument, keyboard, screen, dedicated vision or hand-to-eye coordination on the part of the user to input or retrieve it. That voice mail is nonetheless so widely used is more a function of speech's unique characteristics than a vote of approval on the adequacy of the current technology.

Since speech is a direct record of the user's voice, the urgency, meaning and emotional content is never lost. Similarly, since so much data is first generated in voice and is only later transcribed to text or data, info-text should be the preferred medium for timely data on meetings, speeches and radio broadcasts. Ideally, voice mail should be the preferred mode of communication when traveling, when communicating through time-zones and when accessing timely information which

originated in the spoken word (e.g. minutes of a meeting or lecture). Voice text (i.e. data or text which is spoken by a computer) should be the preferred format for messaging information to be accessed where use of motor skills and vision are not convenient or are impaired such as when driving, operating equipment or engaged in a leisure activity.

The current use of a telephone to access voice messages directly has significantly limited the potential utilization of voice messaging. Real-time transmission of voice messages and info-text makes the recording and retrieval of voice mail, especially from long distances, very costly. The cost and inconvenience involved means that one cannot compose and review voice mail and info-text in a cost efficient manner and at one's own pace. One is limited to a location and situation in which a telephone is accessible and, in the case of a wireless communication link, to a place where wireless transmission is both possible and desirable. In its present state, voice mail is limited to short messages between individuals wishing to communicate in a more substantive fashion at another time (telephone tag). Voice "mail" becomes limited to voice "messaging" because of the cost and inconvenience to both the sender and receiver of listening to lengthy, content-rich "mail" over the phone. Furthermore, the cost of transmitting audio signals in real-time and only when the user has access to a telephone (as opposed to un-attended recording at off-peak hours) makes more commercial use of info text (recorded instructions, recorded travelogues, speech transcripts, articles or books on "tape" etc.) and other innovative advertiser/promotional supported uses of voice-text unfeasible.

Broadly, it is an object of the present invention to provide a dictation device and method which enable a user to compose and review voice mail off-line, from any location, while engaged in any activity, at a leisurely pace, without incurring telephone toll charges and whether a communication link is presently accessible or not.

It is also an object of the present invention to use a telephone link primarily as a communications link for high

speed transmission of pre-recorded material and control codes to facilitate that transmission, thereby limiting the use of a telephone and telephone line for voice messaging as a recording or playback device.

It is also an object of the present invention to provide a protocol whereby pre-message handshaking occurs between the dictation device and a host computer to conform the digitized voice signal to one of the standard voice compression protocols to facilitate high speed transmission of voice messages.

The invention provides a low-cost, portable recording and playback dictation device which permits the user to record, edit, play and review voice messages including audio-text, text-to-speech and other audio material which may be received from, and subsequently transmitted to, a remote voice processing or interactive voice response (IVR) host computer over a communication link, such as the public switched telephone system. A preferred device contains its own power source, integrated circuitry and control buttons to permit the localized recording, editing, storage and playback of audio signals through a built-in speaker, microphone and removable memory card. The device also contains a standard RJ-11 telephone jack, modem chip set and DTMF tone decoder to permit the transmission and control of audio signals to and from a host computer. The device contains circuitry which permits it to transmit and receive audio signals at a rate substantially faster than originally recorded.

The invention also relates to a method and software utility which enables the user to control the delivery and/or transmission of audio data between the device and a host computer by a simple method such as DTMF encoded delivery commands, or spoken instructions, sent by the user and received by and responded to by the voice processing host computer. In response to control codes issued by the user, the utility permits selected voice messages to be retrieved directly into the device or forwarded to the device, which may be located at a remote site and left unattended while connected to a communication link.

It is a feature of the present invention that a recording device may be left connected to a communication link and a voice mail user is able to have voice mail forwarded to him at off-peak hours, when telephone rates are lowest and when excess capacity on incoming lines is available. The recording device is programmed to respond to control codes issued by the host voice processor to enable automatic and unattended recording of selected incoming voice messages.

It is a further feature of the present invention that both senders and recipients of voice messages are able to manage voice messages efficiently for transmission to a recording device through a simple method such as DTMF encoded delivery commands, or spoken instructions, provided to the voice processing host computer. A sender of voice mail is able to annotate a voice message with a message file title and then leave a more substantive voice file either in the receiver's voice mail box, on his own system or at a service bureau for the intended recipient to retrieve using a code given in the message file title. The intended recipient can scan his messages by title, date, length and priority level while on the phone and tag those messages he wishes to have transmitted to his (and possibly additional) recording device(s). Similarly a user requesting pre-recorded audio text or audio signals may respond to prompts which enable him to designate any telephone number, and the best calling time, to which the unattended recorded device is or will be connected and to which audio text could be forwarded. In some cases, the user requesting pre-recorded audio text or audio signals will have the recording device connected to the very line from which he is making his request, in which case he will have the option to have the requested material transmitted directly to his recording device without dropping carrier.

It is also a feature of the present invention that an interface port such as a standard RJ-11 telephone jack is provided so that the recording device may be connected between a telephone set, computer, cellular phone or personal digital assistant and a communication link to enable the user to select and retrieve voice files while using any of those devices.

It is also a feature of the present invention that circuitry is provided for the digital conversion and compression of the analog voice signals recorded in the memory of a dictation device to permit high density storage and high speed transmission of digitized voice. Similarly, circuitry is provided for the analog conversion and natural sounding playback of previously stored or received digitized voice.

It is also a feature of the present invention that there may be provided a public terminal e.g. in a manner similar to an automated teller machine and located at places such as airports where a user could connect his recording device and select voice messages to be retrieved and transmitted directly by the recording device.

Brief Description of the Drawing

The foregoing, as well as the other objects, features and advantages of the present invention will be understood more completely from the following detailed description of a preferred embodiment, with reference being had to the accompanying drawing, in which:

Figure 1 is a schematic block diagram of a preferred personal audio message processor embodying the present invention; and

Figures 2-6 are flowcharts illustrating how certain processing is performed in the apparatus of Fig. 1.

Detailed Description

Figure 1 is a schematic block diagram of a presently preferred Personal Voice Server (PVS) system 10 embodying the present invention. PVS system 10 broadly comprises five main parts: a highly integrated voice chip 12; a modem chip 24 coupled to the voice chip; a flash memory 14 coupled to the voice chip; peripherals such as a microphone 20, a speaker 28, a keyboard 18, and a display 16 coupled to the voice chip; and control software operating a control processor in the voice chip. Although the embodying device is referred to as a voice server, it should be clear that it is equally useful for other types of audio, including music, as well as other signals.

The voice chip is preferably an EV1008 available from EUROM Flashware Solutions, Inc. of Santa Clara, California, but may be any chip providing similar functions and operation. Voice chip 12 provides integrated voice recording, playback and control, managed by the software in accordance with the invention. An internal controller in the voice chip controls the compression of audio, writing and reading of audio data to/from flash memory 14, control of the external modem chip 24 and a standard UART interface. The sampling rate of the chip is controlled by the software.

Flash memory 14 is configured according to the recording time to be available on PVS 10, preferably up to 12 MB of non-volatile flash memory. In a typical situation audio compression will result in a data bandwidth of about 1 KByte per second (about 7kbps). In this mode a memory of 1 MByte will provide 1000 seconds of audio for retransmission.

A microphone 20 and speaker 28 are selected based on quality and size.

The software embedded in the PVS system permits multiple operations by it, such as keying in a command, talking to and recording in the PVS, as well as audio compression either by a scheme on the voice chip 12 (about 8 kbps) or directly by the modem chip 24 (by a standard ADPCM algorithm, to enable 2 bit qauntization and about 14 kbps). The compressed data may either be transmitted directly by the modem 24 or stored by the voice chip in the flash memory 14. Alternatively, another software algorithm may be added for compressing the audio by standard form of data compression used by a service bureau.

A controller in the voice chip 12 executes software that is resident in the flash memory 14. The program can be updated by automatic reloading of the program over a telephone line over which the audio is sent. The core part of the software that handles the modem and the handshake communication is embedded in the kernel program, and the system address base is configured to drive display 16, preferably an LCD display. The system database is configured to read the keyboard 18. Every time a key of the keyboard is pressed, an interrupt is

generated to the controller, which then polls the system data to determine which key was pressed. The software decides what action to perform.

A voice input is provided from microphone 20, through an amplifier 22, to the analog data input of voice chip 12. The controller in the voice chip applies the voice input to an internal ADC (Analog to Digital Converter), reads the output of the ADC, compresses the output data and causes it to be stored in flash memory 14. The voice chip plays back the data when it receives an appropriate command from the keyboard 18 or directly from a telephone line connected to the receiving machine. The data is read back from the flash memory, decompressed, and converted to an analog signal via a DAC (Digital to Analog Converter) in the voice chip 12.

The line output of modem chip 24 is connected through a conventional telephone jack 30, such as an RJ-11, which permits connection to a telephone line. However, it will be appreciated that the modem could also be a cellular or other radio transmission modem. The modem is also connected to the UART interface of voice chip 12. Transmission of previously recorded audio is performed by the controller reading data from flash memory 14, which data is previously compressed audio. This data is sent by the modem to the external telephone line for transmission to the receiver. Prior to this, controlling software dials the required number and waits for the receiving telephone to prepare for the transmission. This is done by a known handshake procedure or communications protocol, such as ZMODEM, KERMIT, or X/Y MODEM. After communication is established, the modem transmits all the bits of the digital audio to the receiver by V.34 standard protocol (28.8 Kbps). These audio bits are extracted by the controller from a predefined location in flash memory, under control of the software. The software has a directory of messages in the flash memory which can be retrieved independently by the controller.

While receiving the messages, the modem sends the received stream of bits to the controller of the voice chip. The controller, by means of software manages the pool of

messages and free space in the flash memory and stores the data bits in the free space of the memory. This data can be either raw data compressed by an identical voice chip or by other voice chips of audio providers (e.g. A personal computer with audio board and compression software). In parallel with this, audio coming from the microphone may be digitized and stored directly and compressed by the voice chip, or it may be compressed by the modem and then re-captured by the UART of the voice chip. This enables storage of audio which contains compatible ADPCM standard compression, as used by the modem chip and many types of hardware.

Speaker 28 and microphone 20 are connected to the voice chip through amplifiers 22 and 26, respectively.

Flow-diagrams are presented in Figs. 2-6 to describe the reception by and transmission of messages to and from the Personal Voice Server (PVS) and all the different operational options for receiving, storing, retrieving, transmitting and playing messages to and from the PVS. This includes receiving compressed messages in digital form and audio signals in analog form either directly from a microphone or through a telephone connection.

For a more complete understanding of the embodiment of Fig. 1, a complete data sheet for the EV1008 VoiceChip™ is attached as Appendix A and is incorporated in this description by reference.

Figure 2 is a flowchart illustrating how the PVS receives previously digitized messages from a central message server which is compatible with the communication protocol used by the PVS (this could be any supported de-facto or proprietary standard, e.g. DSVD (Digital Simultaneous Voice and Data), which is sent via V.34 protocol at 28.8 kbps and which would permit the user to talk while data is being transmitted to his/her PVS.

Operation begins at block 200. At block 210, the modem, in response to a ring, answers the call, completes its handshake procedure, and begins receiving information. Data bits from the modem are received by voice chip 12 at block 212. The voice chip decodes the incoming data at block 214. At

block 216, a test performed to determine whether the operation desired to be performed is storing a previously digitized, incoming message. If not, control switches to the process of Fig. 3. Otherwise, operation continues at block 218, where the incoming data packets are stored in flash memory 14. Upon completion of the entire message (block 220), a test is performed at block 222 to determine whether the memory was filled before the complete message was stored. If not, an acknowledgement is sent to the sender (block 224) that the complete message was received, and control returns to block 200. If the memory was filled up, the PVS stops receiving information (block 226), the central server is notified (block 228), and control returns to block 200.

In packetizing data, a large number of bytes of data are separated into many identically structured packets, which are sent together with synchronization and validity information to withstand errors in transmission. In case of a error, only the required packets are re-sent to the PVS, if that is required. The type of transmission and the protocol between the sender and receiver can be any commonly used computer communications protocol, such as z-modem, v.34 or ppp.

Figure 3 is a flowchart which illustrates the process for retrieving previously digitized and compressed messages from the PVS and transmitting them to a central server. At block 300, a test is performed to determine whether the requested service is retrieval and transmission of a previously digitized, compressed and stored message. If not, control is transferred to the procedure of Fig. 4. If so, the requested data is retrieved from memory at block 310. This data is managed by the controller in voice chip 14. The various messages are grouped as a collection of messages and are described in a compact directory which is managed by the controller. The messages are retrieved from the flash memory by going to its starting location, splitting its contents into packets, and sending the data to the modem. The data packets are sent without compression (block 320), since they have been compressed previously, upon storage. The controller loops through the entire pool of messages (block 330) and sends out

all messages that need to be transmitted (block 330), preferably at a substantially higher rate than would be used for normal digital sound, whereupon control is transfer to the procedure of Fig. 2.

It should be appreciated that this mode of operation makes the PVS a particularly useful and convenient device. The user may carry it with him at all times, recording messages as he wishes, when he wishes. Upon arrival at a convenient location, he can then connect to a telephone line and dispatch all of the accumulated messages at once. This process is particularly efficient, because all of the messages are pre-compressed, organized and packetized by the PVS. Moreover, transmission time and expense are minimized, because the messages are compressed and can be sent in a burst, at the maximum speed of the modem, rather than at the usual transmission rate for digitized voice.

Figure 4 is a block diagram illustrating the routine performed by the controller of voice chip 12 when a received analog audio message is to be recorded. At block 400, a test is performed to determine whether the incoming audio message is from the built-in microphone. If not, control is transferred to the routine of Fig. 5. If so, the audio message is digitized and compressed (block 410) and placed in the working pool of data (block 420). At block 430, a test is performed to determine whether memory was filled before an entire message was stored. If not, the routine is terminated, and control returns to the routine of Fig. 2. If so, recording is disable (block 440), and the operator is notified, as by a warning light, that the memory is full (block 450). Control then reverts to the routine of Fig. 2.

Figure 5 is a block diagram illustrating the routine performed to record analog audio from the telephone line. At block 500, a test is performed to determined whether an audio message being received is from the communications link (telephone line). If not, control is transferred to the routine of Fig. 6. If so, the message is passed through the modem 24 as audio (block 510), and a test is performed at block 520 to determine whether compression is to be performed by the

voice chip. If so, the message is stored in local memory (block 530), recording is stopped, and control is returned to the routine of Fig. 2. If compression is not to be performed by the voice chip, the message is sent to the modem, which compresses it by a standard (ADPCM) algorithm (block 540). The message is then sent back to the voice chip 12 through its UART (block 550), and the voice chip control that causes the message to be stored in flash memory 14 (block 560). Control is then returned to the routine of Fig. 2.

A number of features described to this point are worthy of note. First of all, the PVS can determine whether an incoming signal on the telephone line is digital or analog. It is the analog messages that are subjected to the routine of Fig. 5. Such messages are then digitized and compressed and are stored in the same form as all other messages. Also, the user has the option of having compression performed by the PVS or the modem. This assures compatibility with the ultimate recipient of a message. For example, the recipient may not have a PVS or other device to reverse the compression performed by the PVS. However, he would be likely to be able to decompress a message compressed by the modem.

Figure 6 is a block diagram of the routine performed by the voice chip controller to play stored audio through the built-in speaker. At block 600, the operator selects a message from the pool of messages stored in the device. At block 610, a test is performed to determine whether stored message to be read was originally compressed by the voice chip. If not, control is transferred to block 620. If so, the message is read and decompressed using the voice chip (block 630), and the decompressed message is applied to the digital-to-analog converter (DAC) in the voice chip (block 640). The message is then played via the built-in speaker 28 through the amplifier 26 (block 650), and control is returned to the routine of Fig. 2.

If the stored message was not originally compressed by the voice chip, a test is performed at block 620 to determine whether the stored message was originally compressed by the modem chip. If not, the user is notified (block 660),

and control is returned to the routine of Fig. 2. If so, the message is read by the controller (block 670), and it is then sent to the modem to be decompressed and then returned from the modem to memory 14 through the UART port of voice chip 12 (block 680). Control is then transferred to block 640, and playback is handled in the same manner as a message originally compressed by the voice chip.

Although a preferred embodiment of the invention has been disclosed for illustrative purposes, those skilled in the art will appreciate that many additions, modifications, and substitutions are possible, without departing from the scope and spirit of the invention as defined in the accompanying claims.

EUROM
FlashWare Solutions

VoiceChip™

VoiceChip™ EV1008 Highly-Integrated Voice Recorder

- Implements efficient data compression algorithm - Stores up to 20 min. of voice data in 1 MByte of external memory
- File system to manage voice files
- Real Time Clock with alarm capability
- On-chip controller runs embedded or external software
- Addresses Flash memory for non-volatile data storage
- On-chip Analog to Digital Converter (ADC) for voice recording
- On-chip Digital to Analog Converter (DAC) for playback
- Serial interface via on-chip UART or I^2C bus
- Built-in 4-digit LCD driver
- Integrated keyboard support - up to 16 keys
- Direct read and write access to Flash memory from external system
- Sleep mode for low power consumption
- XIP - Execute in place from Flash memory
- Watchdog timer

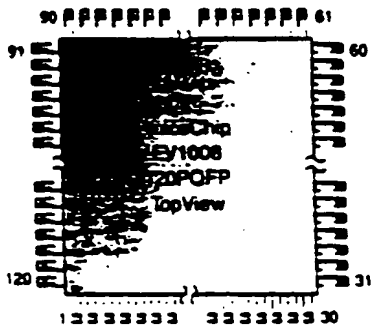

Figure 1. VoiceChip Outline Diagram

Pin Name	Description	Pin Name	Description
RST#	Reset	FA0-FA7	Flash address bus [7:0]
HEMUL	Hardware Emulation	FAD8-FAD15	Flash address/data bus [15:8]
RCI	RC clock input	FA16-FA20	Flash address bus [20:16]
RCO	RC clock output	FCE0#-FCE3#	Flash chip enable bus
XTALI	Crystal clock input	ERCE#	External ROM chip enable
XTALO	Crystal clock output	ERACE#	External RAM chip enable
XT32KI	32.10-Hz Crystal clock input	FOE#	Flash output enable
XT32KO	32.10-Hz Crystal clock output	FWE#	Flash write enable
SD0-SD7 / KEY0-KEY7	System data bus / Keyboard control bus	SDIN	UART Serial Data In
SA0-SA23 / LCD0-LCD23	System address bus / LCD control bus [23:0]	SDOUT	UART Serial Data Out
SCE# / LCD26	System chip enable / LCD control bus [26]	SCL	I^2C Serial Clock
SOE# / LCD24	System output enable / LCD control bus [24]	SDA	I^2C Serial Data
SWE# / LCD25	System write enable / LCD control bus [25]	GPIO0-GPIO7	General Purpose I/O [7:0]
LCD27	LCD control bus [27]	ADCIN	Analog to Digital Converter input
BPCLK	LCD backplane clock	DACOUT	Digital to Analog Converter output
FD0-FD7	Flash data bus [7:0]		

Table 1. VoiceChip Pin Description

APPENDIX A
A-1

GENERAL DESCRIPTION

VoiceChip is a voice recorder chip that provides an integrated solution to voice applications. The combination of many functional units integrated in one device with many operating modes and complete user control through an on-chip controller results in a flexible, low-cost solution for a broad range of applications. VoiceChip uses an external flash memory array with a maximum capacity of 12 MB for data storage.

The heart of VoiceChip is an 8-bit RISC controller that controls the operation of all of the VoiceChip functional units as well as communication with external systems. An internal 2Kx8 ROM and a 256x8 RAM are dedicated to the controller. Alternately, the controller can access external memory devices for program and data storage.

VoiceChip includes two serial ports, a UART port and an I²C Bus port, that provide external access to VoiceChip and the flash memory array. A system bus provides parallel access to the flash array. In addition, VoiceChip integrates an LCD controller and a keyboard controller that use the system bus pins. On board the VoiceChip are a 10-bit Analog to Digital converter and an 8-bit Digital to Analog converter that replace the codec that is required by comparable solutions. Other VoiceChip functional units include a timer, a Real-Time Clock and an alarm unit. There are 8 general-purpose I/O pins that can be used to poll or drive system signals.

Accompanying VoiceChip is a library of application routines that include voice compression algorithms, flash memory file management and support for VoiceChip's functional blocks. The VoiceChip controller is supported by an assembler, a debugger and a software emulator. These tools are PC-based, and are supplied with VoiceChip. VoiceChip also has a hardware emulation mode to enable in-system debug.

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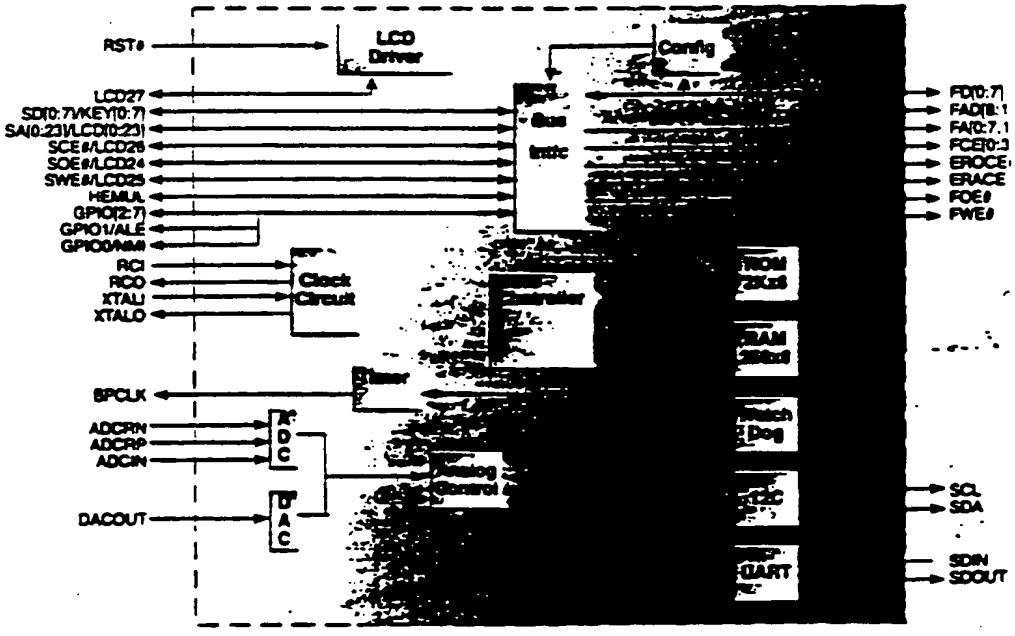


Figure 2. VoiceChip Block Diagram

EUROM Ltd. 16 Preliminary

VoiceChip™

EV1008
Highly-Integrated Voice Recorder

- Implements efficient data compression algorithm - Stores up to 20 min. of voice data in 1 MByte of external memory
- Real-time clock with alarm capability
- On-chip controller runs embedded or external software
- Addresses up to 12 MBytes of Flash memory for non-volatile data storage
- On-chip Analog to Digital Converter (ADC) for voice recording
- On-chip Digital to Analog Converter (DAC) for playback
- Serial interface via on-chip UART or I²C bus
- Built-in 4-digit LCD driver
- Integrated keyboard support - up to 16 keys
- Direct read and write access to Flash memory from external system
- Sleep mode for low power consumption

GENERAL DESCRIPTION

VoiceChip™ is a voice recorder chip that provides an integrated solution to voice applications. The combination of many functional units integrated in one device with many operating modes and complete user control through an on-chip controller results in a flexible, low-cost solution for a broad range of applications.

The heart of VoiceChip is an 8-bit controller that controls the operation of all of VoiceChip's functional units as well as communication with external systems. The controller executes instructions from a 2 KByte internal ROM. VoiceChip also includes 256 bytes of internal RAM that is used by the controller for temporary storage and data buffering. VoiceChip can be configured so that the controller executes software from an external memory device. In addition, the internal RAM may be replaced by a larger external device.

The internal ROM contains the basic operating software for the controller. This software configures VoiceChip to operate as a digital data recorder that accepts commands and data via a UART serial port or via an I²C Bus serial interface port. Accompanying VoiceChip is a library of macros that support VoiceChip's peripheral blocks such as the A/D converter and implement the voice compression algorithm. These routines are not included in the internal ROM but may be run from an external memory device.

VoiceChip has two external busses. The flash bus can access up to six 2 MByte flash memory devices to provide a total capacity of 12 MBytes of flash memory. The system bus allows direct system access to the 12 MByte flash address space. The system bus is accessed through a microprocessor-compatible interface. VoiceChip has two serial interfaces - an I²C Bus interface and a standard UART serial interface. VoiceChip has a sleep mode that reduces power

consumption. The analog portion of the device includes a 10-bit ADC, and an 8-bit DAC. The sampling rate of the ADC can be varied under the control of the controller. This allows for variable compression rates.

VoiceChip can be configured in a stand-alone configuration where the system bus pins can be configured to directly interface to a 16-key keyboard and to drive a 4-digit LCD display. The keyboard can be used to control VoiceChip's operation in the stand-alone configuration. A programmable timer generates the backplane clock for the LCD display as well as internal interrupts that are serviced by the controller.

VoiceChip is supported by a macro library and compiler. The macro library includes the VoiceChip
voice compression algorithm, the flash message and file system, and drivers for the VoiceChip peripheral blocks. The macro compiler builds a specific application from the macro library.

OUTLINE DIAGRAM

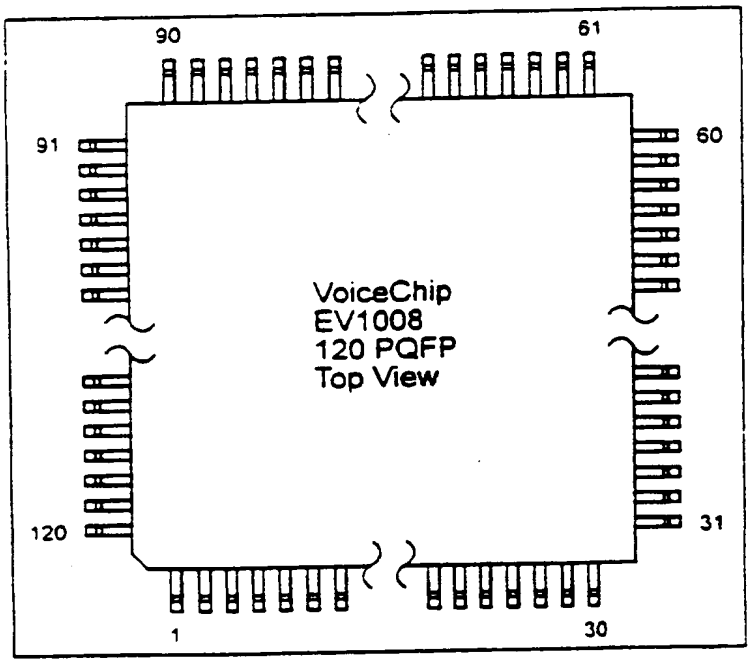


Figure 1. VoiceChip Outline Diagram

PIN DESCRIPTION

Table 1 presents the pin name and pin number of each of the VoiceChip pins. Pins whose names end with '#' are active low.

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	FA0	31	FD7	61	NC	91	DACOUT
2	FA1	32	FD6	62	SA20 / LCD20	92	DACRN
3	FA2	33	FD5	63	SA21 / LCD21	93	DACRP
4	FA3	34	FD4	64	SA22 / LCD22	94	ADCIN
5	FA4	35	FD3	65	SA23 / LCD23	95	AGND
6	FA5	36	FD2	66	GND	96	FCE3#
7	FA6	37	FD1	67	VDD	97	FCE4#
8	FA7	38	FD0	68	GND	98	FCE5#
9	FAD8	39	GND	69	VDD	99	GPIO0 / NMI
10	FAD9	40	VDD	70	SOE# / LCD25	100	GPIO1 / ALE
11	FAD10	41	SA0 / LCD0	71	SWE# / LCD26	101	GPIO2
12	FAD11	42	SA1 / LCD1	72	SCE# / LCD24	102	GPIO3
13	FAD12	43	SA2 / LCD2	73	LCD27	103	GPIO4
14	GND	44	SA3 / LCD3	74	RCI	104	GPIO5
15	VDD	45	SA4 / LCD4	75	XTALI	105	GPIO6
16	GND	46	SA5 / LCD5	76	XTALO	106	GPIO7
17	VDD	47	SA6 / LCD6	77	RCO	107	GND
18	FAD13	48	SA7 / LCD7	78	SD0 / KEY0	108	VDD
19	FAD14	49	SA8 / LCD8	79	SD1 / KEY1	109	SDIN
20	FAD15	50	SA9 / LCD9	80	SD2 / KEY2	110	HEMUL
21	FA16	51	SA10 / LCD10	81	SD3 / KEY3	111	SCL
22	FA17	52	SA11 / LCD11	82	SD4 / KEY4	112	SDA
23	FA18	53	SA12 / LCD12	83	SD5 / KEY5	113	EROCE#
24	FA19	54	SA13 / LCD13	84	SD6 / KEY6	114	ERACE#
25	FA20	55	SA14 / LCD14	85	SD7 / KEY7	115	BPCLK
26	FCE0#	56	SA15 / LCD15	86	NC	116	SDOUT
27	FWE#	57	SA16 / LCD16	87	NC	117	XT32KO
28	FOE#	58	SA17 / LCD17	88	AVDD	118	XT32KI
29	FCE1#	59	SA18 / LCD18	89	ADCRP	119	GND
30	FCE2#	60	SA19 / LCD19	90	ADCRN	120	RST#

Table 1. VoiceChip Pin List

Table 2 presents a description of each of the VoiceChip pins.

Pin Name	Direction	Description
RST#	Input	Reset. Initializes VoiceChip. While the reset input is active, VoiceChip samples the Flash data bus to determine its operating mode.
HEMUL	Bi-directional	Hardware Emulation. During reset, HEMUL is sampled. If it is high, VoiceChip enters hardware emulation mode. In hardware emulation mode, when VoiceChip reaches a breakpoint, HEMUL goes high.
RCI	Input	RC clock input. Clock input that drives the VoiceChip clock from an external RC circuit. The VoiceChip clock can be driven by an external RC circuit or an external crystal.
RCO	Output	RC clock output. Output from VoiceChip that drives the external RC circuit.
XTALI	Input	Crystal clock input. Drives the VoiceChip clock from an external crystal.
XTALO	Output	Crystal clock output. Output from VoiceChip that drives the external crystal.
XT32KI	Input	32.768 KHz crystal clock input. Drives the VoiceChip real-time clock.
XT32KO	Output	32.768 KHz crystal clock output. Output from the circiut that drives the VoiceChip real-time clock.
SD0-SD7 / KEY0-KEY7	Bi-directional	System data bus. In system mode, outputs flash data. Inputs write data during write operations. Enters tri-state mode when the chip or the outputs are deselected. In stand-alone mode, can support a keyboard of up to 16 keys.
SA0-SA23 / LCD0-LCD23	Bi-directional	System address bus. In system mode, selects the byte address for system bus read and write operations. In stand-alone mode, when VoiceChip is configured to drive an LCD display, this drives segments 0-23 of the LCD display. After a breakpoint in hardware emulation, the internal VoiceChip registers are controlled through the system address bus.
SCE# / LCD24	Bi-directional	System chip enable. In system mode, selects VoiceChip for read or write operations. In stand-alone mode, drives segment 26 of the LCD display.
SOE# / LCD25	Bi-directional	System output enable. In system mode, when VoiceChip is selected by the SCE# input, enables the read data on the system data bus. In stand-alone mode, drives segment 24 of the LCD display.
SWE# / LCD26	Bi-directional	System write enable. In system mode, when VoiceChip is selected by the SCE# input, this latches write data into VoiceChip on the rising edge. If SOE# is active, SWE# is ignored. In stand-alone mode, drives segment 25 of the LCD display.
LCD27	Bi-directional	LCD segment 27. During reset, LCD27 is sampled. If it is high, and VoiceChip is configured for stand-alone mode, the system address bus functions as a LCD driver. In stand-alone mode, after reset, LCD27 drives segment 27 of the LCD display.

Table 2. VoiceChip Pin Description

Pin Name	Direction	Description
BPCLK	Output	LCD backplane clock output. Controlled by the on-board programmable timer.
FD0-FD7	Bi-directional	Flash data bus. Returns flash data from the flash devices during read operations and transfers write data to the flash devices during write operations. During power-on, and when the RST# input is activated, VoiceChip samples the Flash data bus. The value that is sampled on the bus determines the VoiceChip operating mode.
FA0-FA7	Output	Flash address bus, bits 0-7. Selects the byte address for flash bus read and write operations. VoiceChip can access flash devices with capacities of up to 2 MBytes.
FAD8-FAD15	Bi-directional	Flash address/data bus, bits 8-15. Selects the byte address for flash bus read and write operations. When VoiceChip is configured for 16-bit instruction fetches, these 8 pins are multiplexed flash address/data pins. In this configuration, the upper 8 bits of the instruction are read in on these pins.
FA16-FA20	Output	Flash address bus, bits 16-20. Selects the byte address for flash bus read and write operations.
FCE0#-FCE5#	Output	Flash chip enable. VoiceChip can select up to six separate flash devices. The total flash address space that can be accessed by VoiceChip is 12 MBytes.
EROCE#	Output	External ROM Chip Enable. This pin is used to select an external memory device for instruction fetches when VoiceChip is configured for an external ROM device. The external ROM device size can be up to 16 KBytes.
ERACE#	Output	External RAM Chip Enable. This pin is used to select an external RAM device for RAM accesses when VoiceChip is configured for an external RAM device. The external RAM device size can be up to 12 KBytes.
FOE#	Output	Flash output enable. Enables the selected flash device for read operations.
FWE#	Output	Flash write enable. Enables the selected flash device for write operations. The write data is latched on the rising edge of FWE#.
SDIN	Input	Serial Data In. UART data input.
SDOUT	Output	Serial Data Out. UART data output.
SCL	Bi-directional	Serial Clock. I^2C serial bus clock signal.
SDA	Bi-directional	Serial Data. I^2C serial bus data signal.
GPIO0 / NMI, GPIO1 / ALE, GPIO2-GPIO7	Bi-directional	General Purpose I/O. These are 8 general purpose bi-directional pins that are available to VoiceChip. When VoiceChip is configured for external interrupts, GPIO0 functions as the NMI input. When VoiceChip is configured for 16-bit instruction fetches, GPIO1 functions as the Address Latch Enable (ALE) signal for FAD8-FAD15.
ADCIN	Input	Analog to Digital Converter Input. Analog input to the 10-bit ADC.
ADCRN	Input	Analog to Digital Converter Negative Reference. Negative reference voltage to the 10-bit ADC.
ADCRP	Input	Analog to Digital Converter Positive Reference. Positive reference voltage to the 10-bit ADC.
DACOUT	Output	Digital to Analog Converter Output. Analog output from the 8-bit DAC.

Table 2 (cont'd). VoiceChip Pin Description

Pin Name	Direction	Description
DACRN	Input	Digital to Analog Converter Negative Reference. Negative reference voltage to the 8-bit DAC.
DACRP	Input	Digital to Analog Converter Positive Reference. Positive reference voltage to the 8-bit DAC.
VDD	Power	Power pins for VoiceChip digital circuitry.
GND	Power	Ground pins for VoiceChip digital circuitry.
AVDD	Power	Power pin for VoiceChip analog circuitry.
AGND	Power	Ground pin for VoiceChip analog circuitry.
NC	–	No Connect. These pins should be left unconnected.

Table 2 (cont'd). VoiceChip Pin Description

BLOCK DIAGRAM

The VoiceChip block diagram is presented in figure 2.

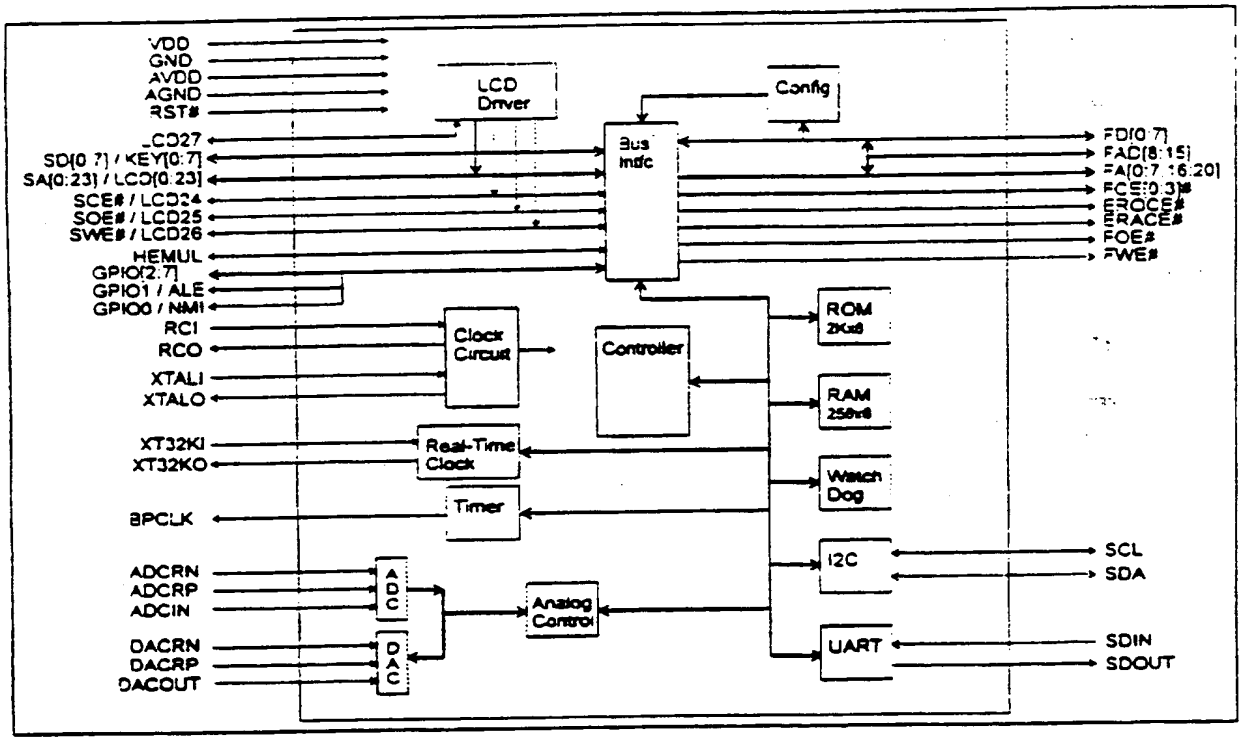


Figure 2. VoiceChip Block Diagram

SYSTEM OPERATION

The VoiceChip system operation is characterized by many different modes of operation. VoiceChip determines its operating mode during reset by sampling the flash data bus. The user can configure VoiceChip to the desired configuration by connecting pull-up or pull-down resistors to the appropriate flash data bits. There are two additional pins, LCD27 and HEMUL that are sampled during reset. LCD27 activates the LCD driver. If HEMUL is active during reset, VoiceChip enters hardware emulation mode after reset.

There are two sources of accesses to the flash memory array in VoiceChip: the on-board controller and the external system bus. The flash array is accessible to only one of the two sources at one time. When the controller has access to the flash array, the system bus cannot access the flash array. When the system bus has access to the flash array, the VoiceChip clock is disabled and the controller is shut down in order to reduce power consumption. This is the VoiceChip sleep mode. The controller wakes up and resumes control of the flash array when it receives the appropriate command on either of the two serial ports. The controller transfers access to the flash array to the system bus either as a result of normal program execution, or when it receives a command on one of the serial ports.

The controller has four possible sources for instruction fetch operations: internal ROM, external flash, external ROM, or RAM. The internal ROM contains a program that allows VoiceChip to function as a digital data logger. Routines from the VoiceChip library and user programs may be stored in the flash memory or in a separate program memory. The program memory is called "external ROM", but it may be any parallel-access memory device. The external ROM size may be up to 16 KBytes. Storing a program in the flash memory provides the advantage of keeping the total component count down to a minimum. However, when a block in the flash memory is erased or when a byte is written to the flash, the entire flash device is unavailable for read operations. Using the external ROM for program storage allows VoiceChip to use the flash memory freely without concern for the effects of erase or write operations on the availability of program data. The controller can also fetch instructions from the RAM. This allows a program to copy a code segment from the flash to RAM, perform an erase or write operation on the flash, and continue program execution from the RAM.

VoiceChip has an 8-bit flash data bus, and instruction fetches are 8-bit operations. In this configuration, pins FAD[8:15] function as flash address pins only. In order to improve the controller performance, VoiceChip can be configured to perform 16-bit instruction fetches. In this case, pins FAD[8:15] function as multiplexed flash address/data pins and GPIO1 is configured as an Address Latch Enable (ALE) pin. ALE is active to latch the flash address bits [8:15] in an external latch.

VoiceChip contains 256 bytes of on-board RAM. The RAM is used by the controller for temporary storage. The RAM can also be used for instruction fetches, as explained above. Alternately, the controller can access an external RAM device in place of the on-board RAM. The external RAM size may be up to 12 KBytes.

VoiceChip has two possible clock sources, an external crystal or an external RC circuit. The crystal provides an accurate clock source, while the RC circuit provides a low-cost solution. Since the RC circuit has limited accuracy, VoiceChip provides the ability to run the internal clock at 1/2 the external oscillator frequency. This provides the VoiceChip internal clock with a 50% duty cycle.

As explained above, VoiceChip enters sleep mode when access to the flash memory is transferred to the system bus. In order to wake up and regain access to the flash bus, the controller must receive a wake-up command sequence on one of the two serial ports. VoiceChip can be configured to grant flash memory access to the system bus immediately after reset. In

this configuration, the VoiceChip clock and controller are disabled at the end of reset, and the system bus has access to the flash memory. The other option is that the controller begins program execution immediately after reset.

VoiceChip can be configured in a stand-alone mode where the system bus can function as a keyboard driver and a LCD display driver. When VoiceChip enters sleep mode in a stand-alone configuration, the LCD display is turned off as well. VoiceChip can be woken up through a command on one of the serial ports as in the system configuration. Additionally, pressing any key on the keyboard will wake up VoiceChip. In order to determine which key is pressed, the controller must poll the system data bus. In this way, the keypad can be used to control VoiceChip in stand-alone mode.

VoiceChip has a hardware emulation mode. In this mode, the user can define two kinds of breakpoints. The first breakpoint is a PC breakpoint which is reached when the controller reaches an instruction whose address matches the defined PC. The second breakpoint is a single-step breakpoint which is reached after every instruction execution. When a breakpoint is reached, HEMUL is asserted high, and the controller halts program execution. At this point, the user has full read and write access to the VoiceChip internal registers via the system address bus. Program execution is resumed by writing to a control register in VoiceChip.

The ADC operation is controlled by the application program. The program determines at what frequency the ADC samples its input and when to read the ADC digital output. Specifically, a program can increase the ADC sampling rate in order to increase the audio quality at the expense of the amount of data that can be stored. Alternately, a program can decrease the ADC sampling rate in order to increase the amount of stored data at the expense of the audio quality.

SYSTEM APPLICATIONS

This section presents some sample system applications of VoiceChip.

Low-Cost Digital Tape Recorder

With the addition of a single flash memory device and two amplifiers, VoiceChip can implement a simple digital tape recorder, as shown in figure 3. In this configuration, the VoiceChip controller executes software that is resident in the external flash memory. The system address bus is configured to drive the 4-digit LCD display. The timer generates the backplane clock for the display. The system data bus is configured to read a 16-key keyboard. Every time a key is pressed, an interrupt is generated to the controller, which then polls the system data bus to determine which key is pressed. The software decides what action to perform at the command of the keyboard. The voice data is input from a microphone to an amplifier and from the amplifier to analog data input of VoiceChip. The controller reads the output of the ADC, compresses the data and stores it in the flash. VoiceChip plays back the data when it receives the appropriate command from the keyboard. The data is read back from the flash, decompressed, and output via the DAC.

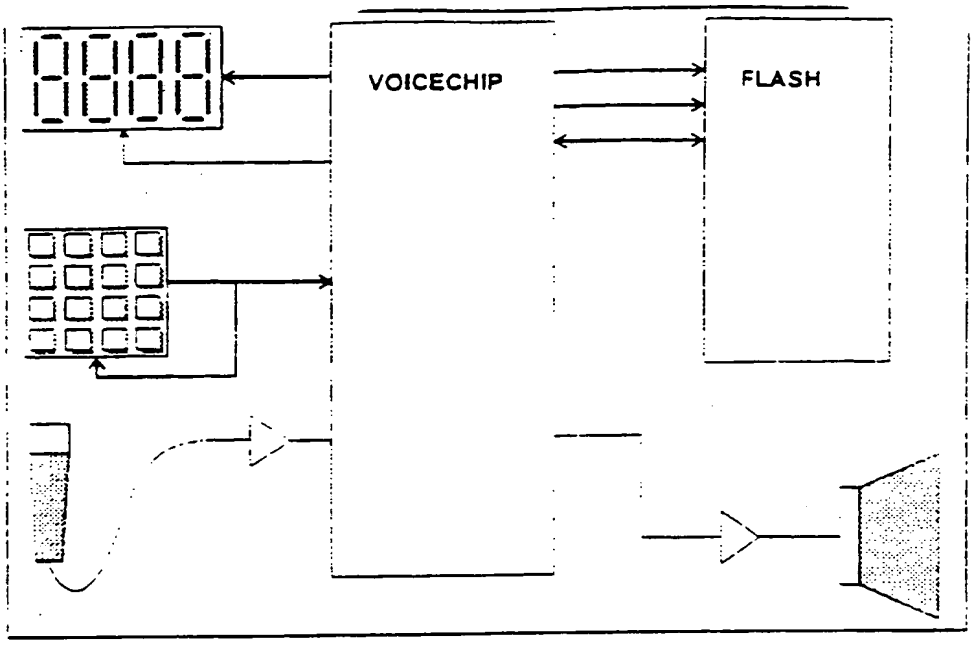


Figure 3. Low-cost Digital Tape Recorder Application

Data Logger

Figure 4 shows VoiceChip configured as a data logger for an analog signal. The flash bus is connected to multiple flash devices for data storage. This application also uses external ROM and external RAM. The controller executes software from the external EPROM and uses the external RAM for temporary storage. VoiceChip accepts commands via the I²C Bus that instruct it when to sample the analog data. The analog data is sampled and stored in the flash without compression. The sampled data is accessed directly from the flash by an external system via the system bus.

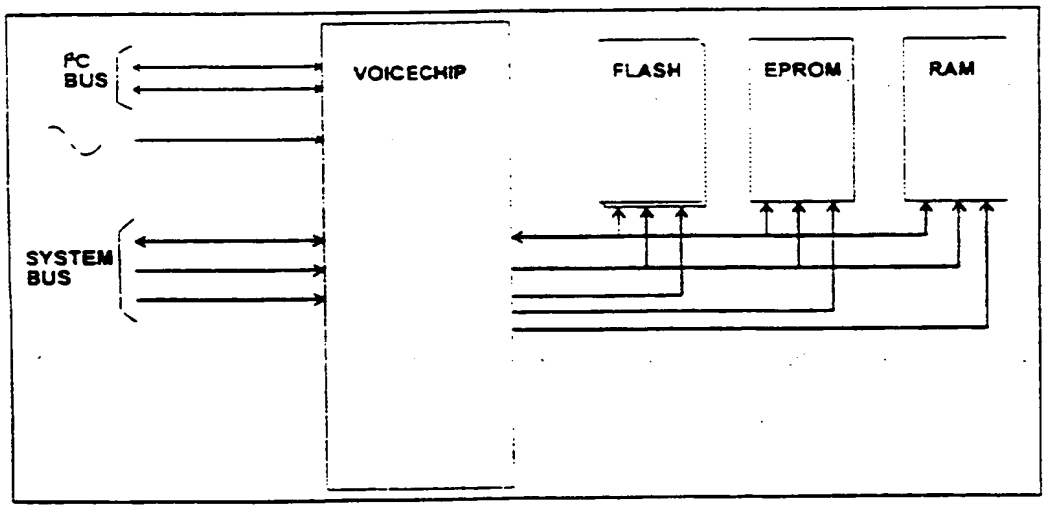


Figure 4. Data Logger Application

Remote Storage Subsystem

The diagram in figure 5 shows VoiceChip configured as a remote storage and display subsystem connected to the serial port of a PC. The PC serial port is connected through a level-shifting buffer to the VoiceChip UART. The PC downloads commands and data to VoiceChip. VoiceChip stores the data in the flash. In response to the commands that are transmitted by the PC. VoiceChip drives an LCD display and outputs the flash data as analog data through the DAC.

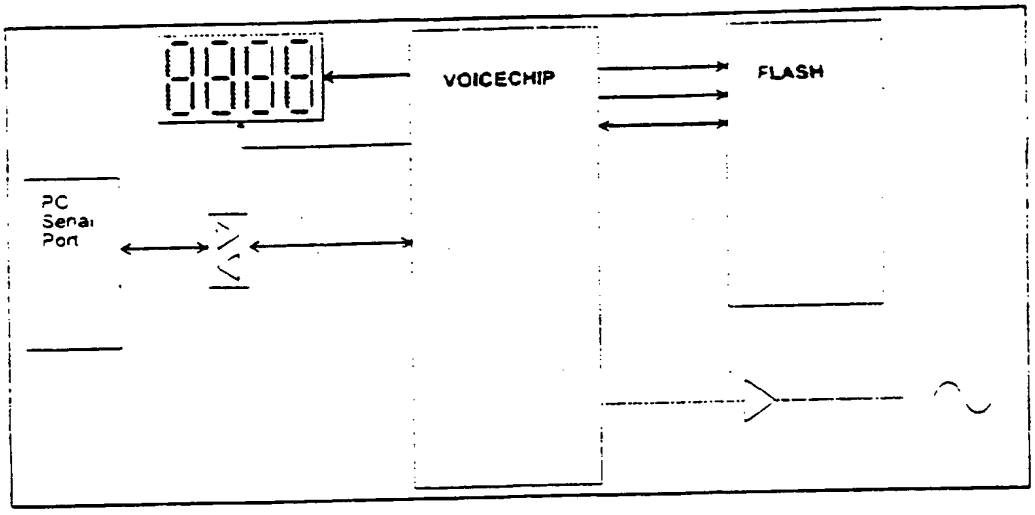


Figure 5. Remote Storage Application

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Temperature Under Bias	-10°C to +80°C
VCC Voltage with Respect to Ground	-0.5V to +7.0V
Voltage on Any Pin with Respect to Ground	-0.5V to VCC+0.5V
Output Short Circuit Current	20 mA

OPERATING RANGES

Operating Temperature	0°C to +70°C
VCC Supply Voltage	+4.5V to +5.5V

DC CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
I_{LI}	Input Leakage Current		± 50	nA	VCC = 5.5V V_{IN} = 0V to 5.5V
I_{LO}	Output Leakage Current		± 70	nA	VCC = 5.5V
I_{CC1}	VCC Active Current		TBD		
I_{CC2}	VCC Standby Current		TBD		
V_{IL}	Input Low Voltage		0.8	V	VCC = 4.5V
V_{IH}	Input High Voltage	2.0		V	VCC = 5.5V
V_{OL}	Output Low Voltage		0.5	V	I_{OL} = 5.5 mA VCC = 4.5V
V_{OH}	Output High Voltage	4.0		V	I_{OH} = -5.5 mA VCC = 4.5V

APPENDIX A
A-13

WHAT IS CLAIMED:

1. An apparatus for communication of audio signals in analog and digital form and for storage of the same, comprising:

digital storage means;

a connection to a communication channel;

a modem having an input coupled to said connection and a digital output;

an analog-to-digital converter having an output coupled to said storage means; and

a controller coupled to said storage means and said modem, and comprising:

means for detecting whether a signal on said connection is an analog or digital audio signal;

routing means controlled by said means for detecting and coupled to said modem, said storage means and said analog-to-digital converter, upon said detecting means detecting a digital signal said routing means causing the output of said modem to be coupled to said storage means, upon said detecting means detecting an analog signal said routing means causing said modem to bypass the signal on said connection and coupling the same to said analog-to-digital converter for subsequent storage in said storage means.

2. The apparatus of Claim 1 further comprising the coupling to said storage means being effected through a device which compresses the signal prior to storage.

3. The apparatus of Claim 1 wherein said modem is of the type including means for compressing a digital signal, the coupling to said storage means being effected through a compression router which connects said means for compressing and directs the resulting signal to said storage means.

4. The apparatus of Claim 1 wherein said modem is of the type including means for compressing a digital signal, said apparatus further comprising a device which compresses a digital signal, the coupling to said storage means being effected through a compression routing means for selectively connecting one of said device and said means for compressing and for directing the resulting signal to said storage means.

5. The apparatus of Claim 1:

said modem having an analog input and output coupled to said connection and a digital input and output; and

said controller further comprising:

means for assembling digital messages stored in said storage means into a packetized data stream containing data and control bits; and

means for coupling said packetized data stream to the digital input of said modem for transmission over said communication channel.

6. An apparatus as in claim 5 wherein said controller causes said modem to transmit said packetized data stream at a rate that is substantially higher than the transmission rate of digitized voice.

7. An apparatus for communication of audio signals in analog and digital form and for storage of the same, comprising:

digital storage means;

a connection to a communication channel;

a modem having an analog input and output coupled to said connection and a digital input and output; and

a controller coupled to said storage means and said modem, and comprising;

means for assembling digital messages stored in said storage means into a packetized data stream containing data and control bits; and

means for coupling said packetized data stream to the digital input of said modem for transmission over said communication channel.

8. An apparatus as in claim 7 wherein said controller causes said modem to transmit said packetized data stream at a rate that is substantially higher than the transmission rate of digitized voice.

9. A method for communication of audio signals in analog and digital form over a communication channel and for storage of the same, comprising the steps of:

detecting whether a signal on said channel is an analog or digital audio signal;

upon detecting a digital signal on said channel, storing in a digital storage means the output of a modem, said modem being of the type having an input coupled to said channel and a digital output;

upon detecting an analog signal on said channel, converting the same from analog to digital form and storing the converted signal in a digital storage means.

10. The method of Claim 9 wherein prior to either of said storing steps said signal is compressed.

11. The method of Claim 10 wherein said modem is of the type including means for compressing a digital signal, said signal being compressed by being connected to said means for compressing and the resulting signal being stored in said storage means.

12. The method of Claim 9 performed with a modem of the type having an analog input and output coupled to said channel and a digital input and output and further comprising the steps of:

assembling digital messages stored in said storage means into a packetized data stream containing data and control bits; and

coupling said packetized data stream to the digital input of said modem for transmission over said communication channel at a rate that is substantially higher than the transmission rate of digitized voice.

13. A method for communication of audio signals in analog and digital form over a communication channel and for storage of the same, said method being performed with a modem of the type having an analog input and output coupled to said channel and a digital input and output and comprising the steps of:

assembling digital messages stored in a storage means into a packetized data stream containing data and control bits; and

coupling said packetized data stream to the digital input of said modem for transmission over said communication channel at a rate that is substantially higher than the transmission rate of digitized voice.

14. A portable device which permits the user to record, edit, play and review voice messages and other audio material which may be received from, and subsequently transmitted to, a remote aparatus a communication link, comprising:

a receptacle for a power source;

integrated circuitry for localized recording, editing, storage and playback of audio signals powered from said receptacle;

non-volatile storage means, access to which is controlled by said integrated circuitry;

a built-in speaker and microphone coupled with said integrated circuitry for audible playback and local input, respectively, of audio;

a modem chip set coupled with said integrated circuitry;

a modular telephone jack coupled to said modem chip set;

the integrated circuitry operating the device so as to transmit and receive audio signals at a rate substantially faster than originally recorded.

15. A device in accordance with claim 14 wherein said integrated circuitry includes a module that is operative to permit distinguishing between analog and digital signals received on the communication link, the analog signals being presented to said integrated circuitry without being processed by said modem chip.

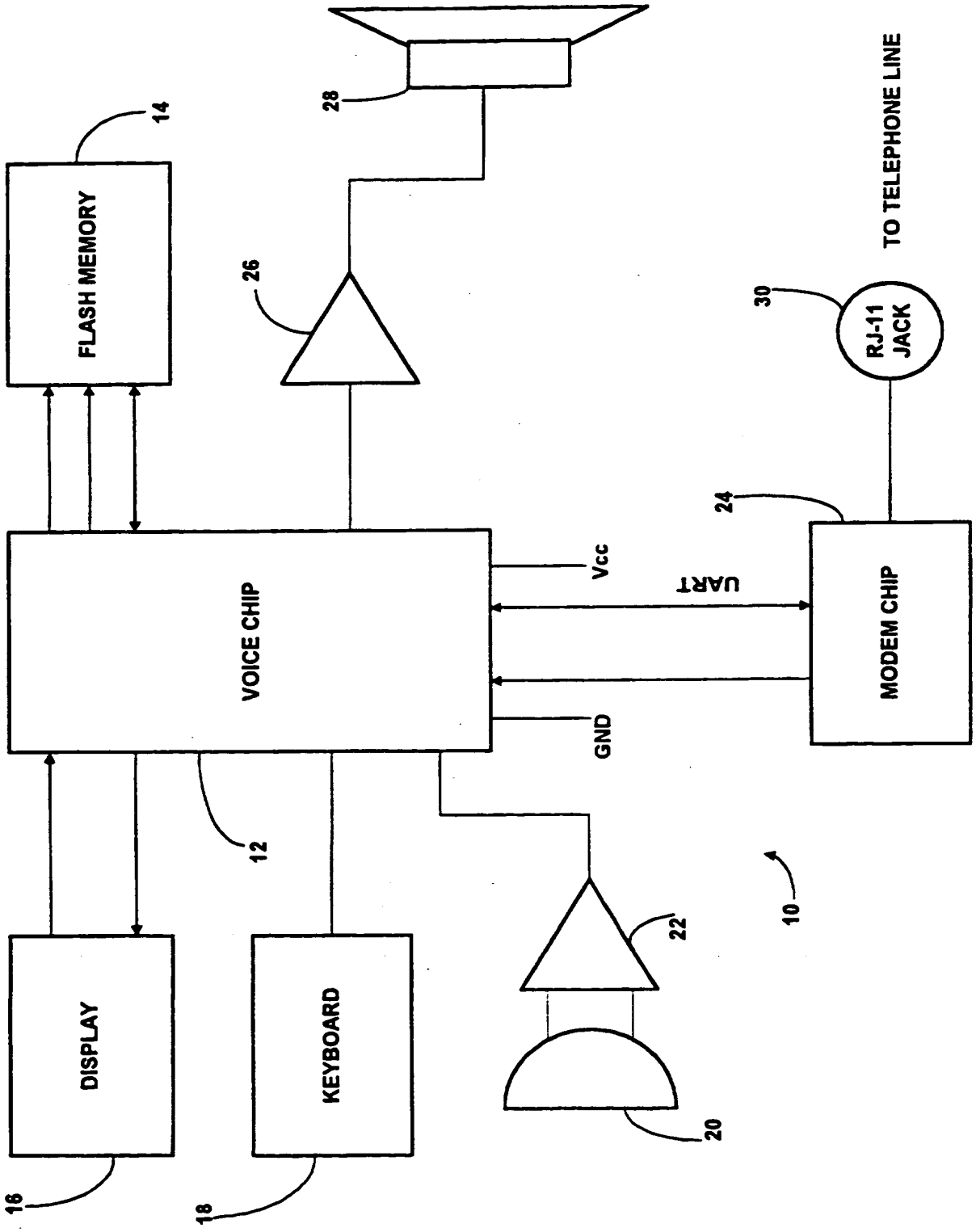
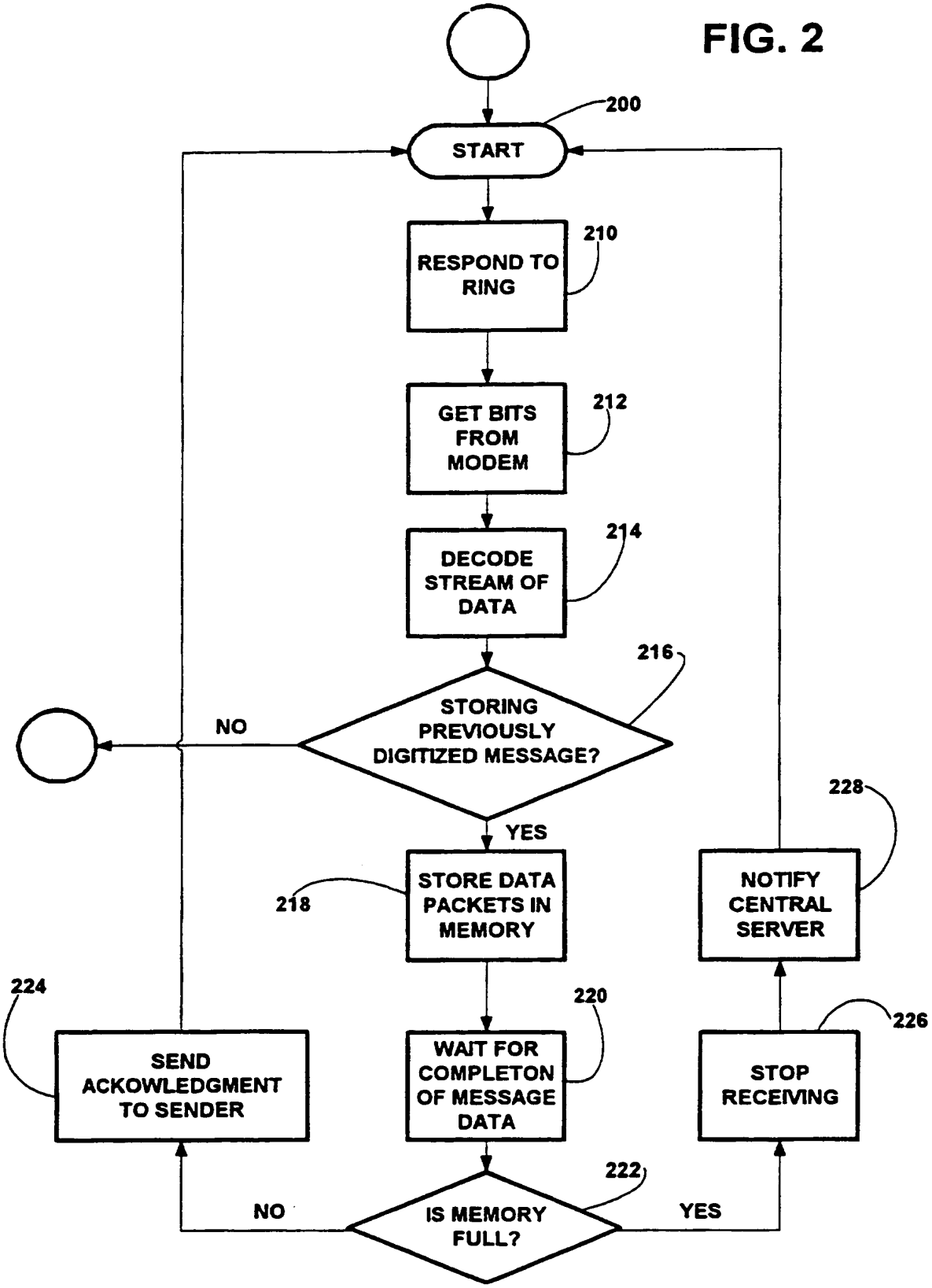

FLASH MEMORY
14
28
26
TO TELEPHONE LINE
30
RJ-11 JACK
24
VOICE CHIP
Vcc
UART
MODEM CHIP
GND
12
10
22
DISPLAY
KEYBOARD
20
16
18

FIG. 1

FIG. 2


200
START
210
RESPOND TO RING
212
GET BITS FROM MODEM
214
DECODE STREAM OF DATA
216
STORING PREVIOUSLY DIGITIZED MESSAGE?
NO
YES
218
STORE DATA PACKETS IN MEMORY
220
WAIT FOR COMPLETON OF MESSAGE DATA
222
IS MEMORY FULL?
NO
YES
224
SEND ACKOWLEDGMENT TO SENDER
226
STOP RECEIVING
228
NOTIFY CENTRAL SERVER

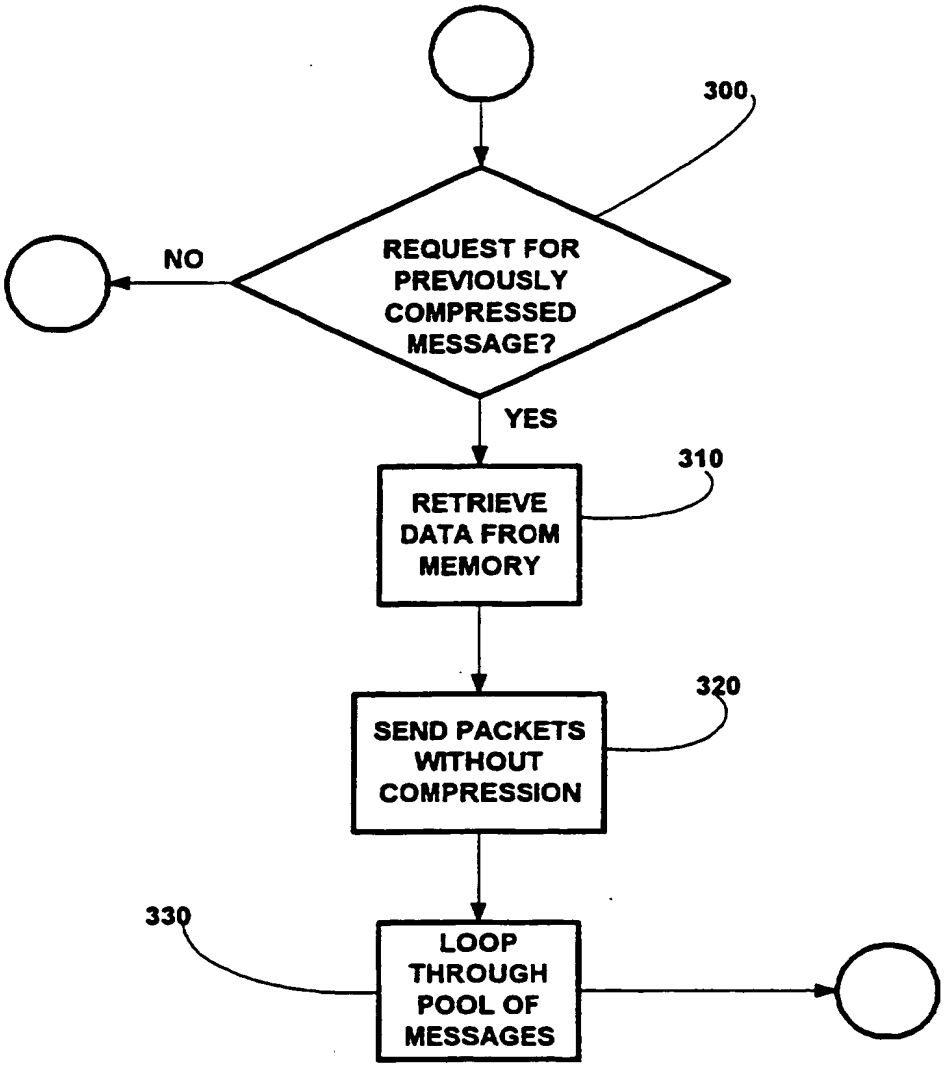

300
REQUEST FOR PREVIOUSLY COMPRESSED MESSAGE?
NO
YES
310
RETRIEVE DATA FROM MEMORY
320
SEND PACKETS WITHOUT COMPRESSION
330
LOOP THROUGH POOL OF MESSAGES

FIG. 3

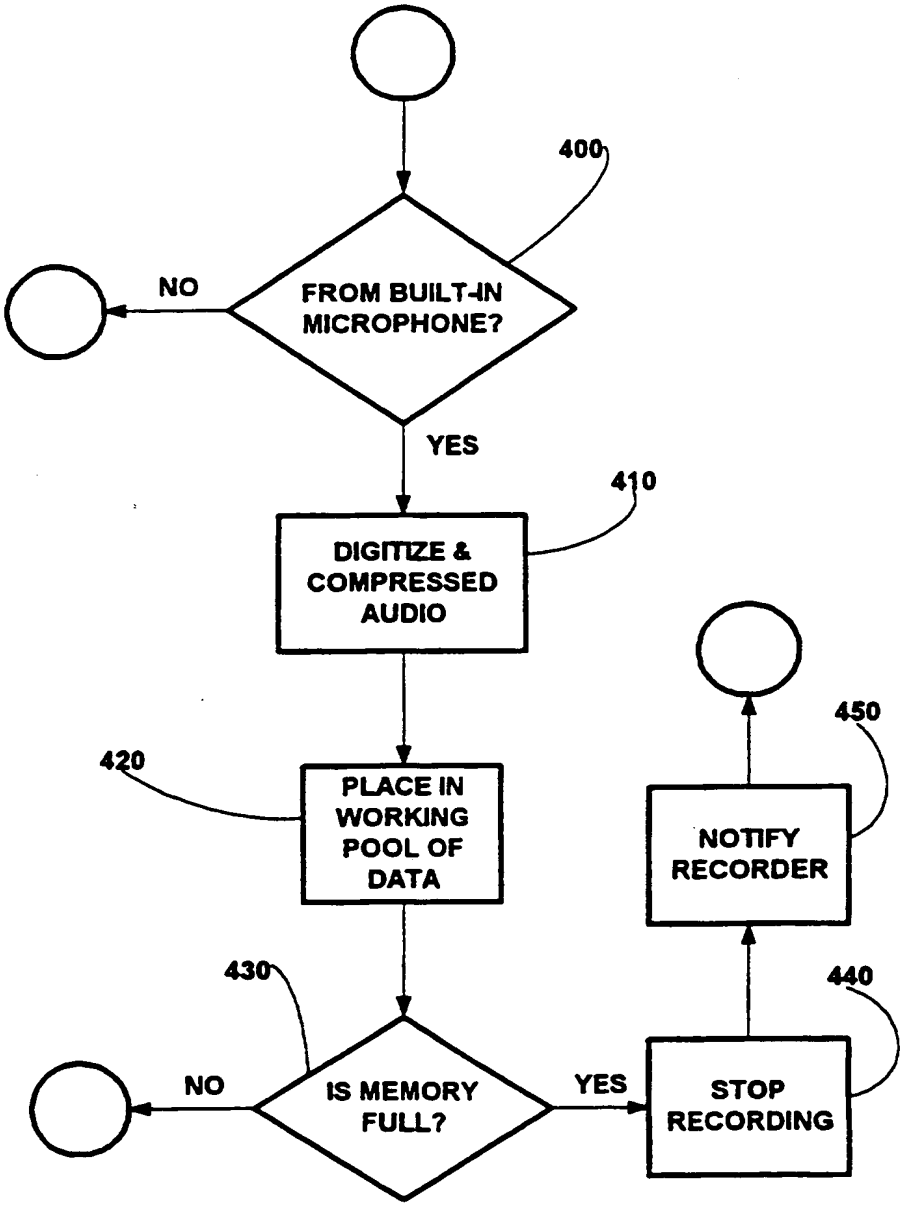


FIG. 4

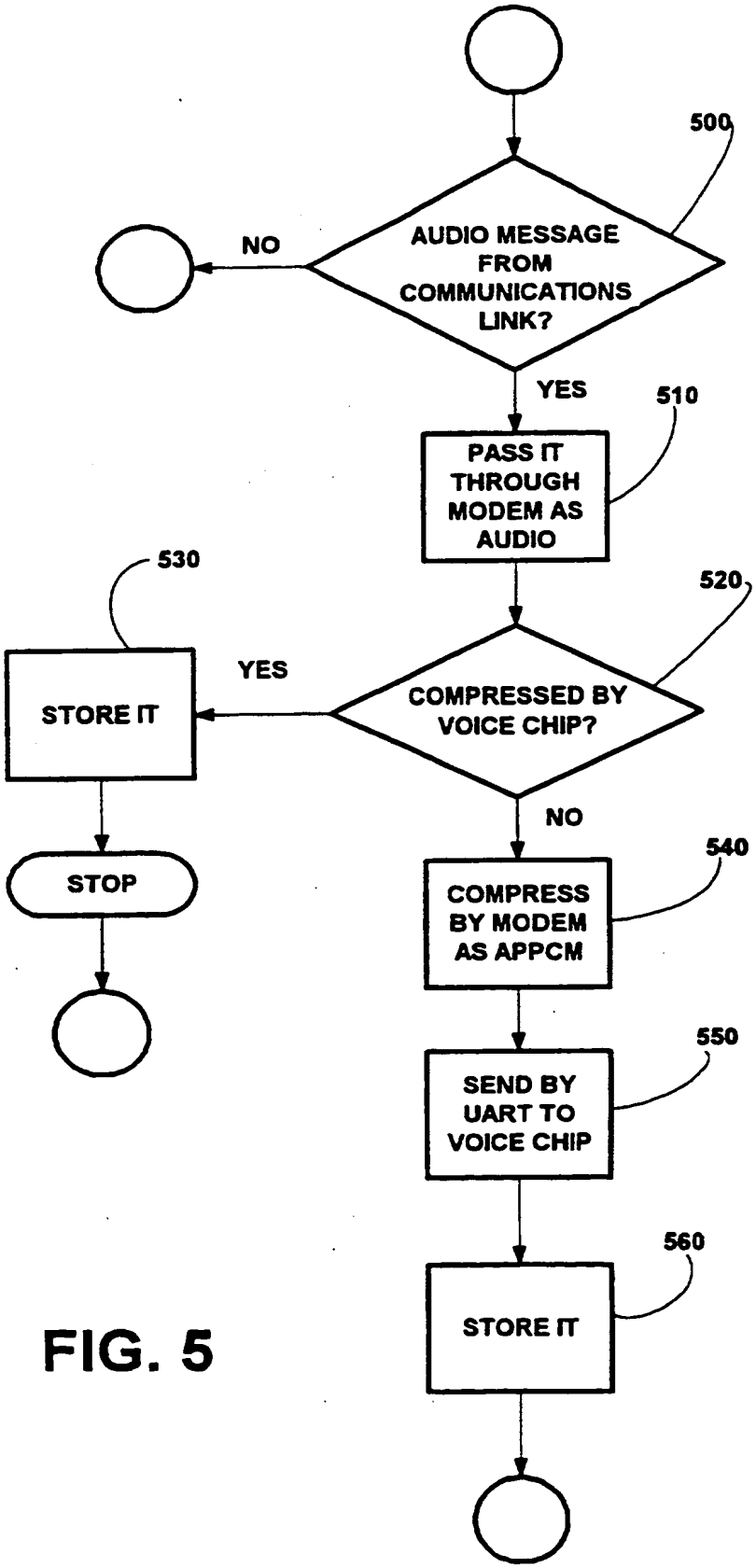
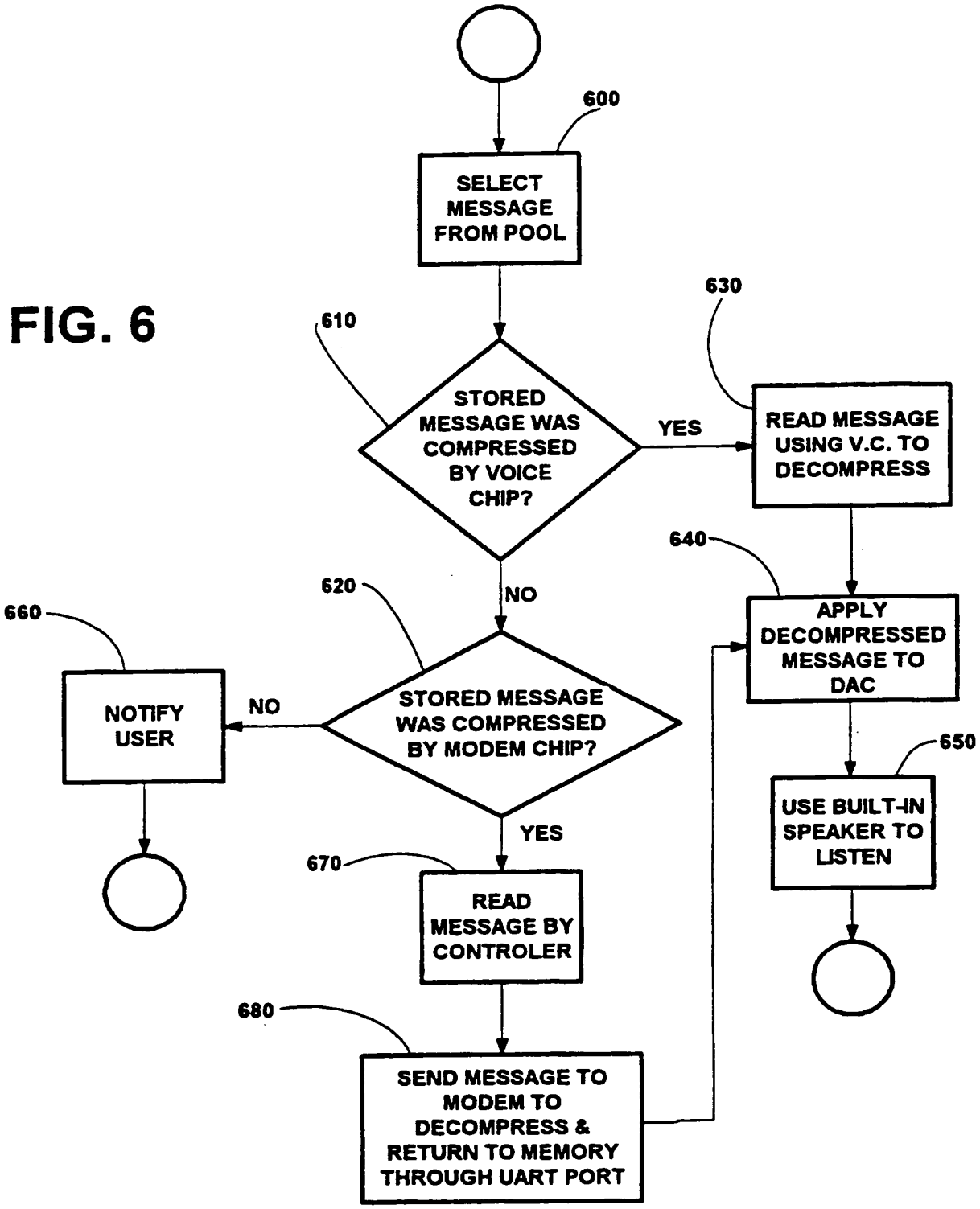

500
AUDIO MESSAGE FROM COMMUNICATIONS LINK?
NO
YES
510
PASS IT THROUGH MODEM AS AUDIO
520
COMPRESSED BY VOICE CHIP?
YES
530
STORE IT
STOP
NO
540
COMPRESS BY MODEM AS APPCM
550
SEND BY UART TO VOICE CHIP
560
STORE IT

FIG. 5

FIG. 6



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/17419

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H03M 7/30

US CL : 395/2.94, 2.1; 379/88;341/50

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 395/2.94, 2.1; 379/88;341/50

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

none

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Please See Extra Sheet.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,132,988 A (FISHER ET AL) 21 July 1992, Title, abstract, fig.2, col. 9.	1-6, 9-12
Y	US 5,451,942 A (BEARD ET AL) 19 September 1995, title, abstract, fig 2, col.3, lines 27-29	1-6, 9-12
Y,P	US 5,508,733 A (KASSATLY) 16 April 1996, fig.1, fig.43, col.51, col.52.	1-6, 9-12
A	US 5,430,661 A (FISHER ET AL) 04 July 1995.	1-6, 9-12
A	US 4,640,991 A (MATTHEWS ET AL) 03 February 1987.	1-6, 9-12
A	US 4,602,129 A (MATTHEWS ET AL) 22 July 1986.	1-6, 9-12

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be part of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 12 FEBRUARY 1997	Date of mailing of the international search report 18 MAR 1997
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer ALLEN MACDONALD Telephone No. (703) 305-9600

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/17419

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5,325,238 A (STEBBINGS ET AL) 28 June 1994.	1-6, 9-12
A	US 5,251,261 A (MEYER ET AL) 05 October 1993.	1-6, 9-12
A	US 5,424,735 A (ARKAS ET AL) 13 June 1995.	1-6, 9-12

Form PCT/ISA/210 (continuation of second sheet)(July 1992)*

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/17419

B. FIELDS SEARCHED
Electronic data bases consulted (Name of data base and where practicable terms used):

Maya search, APS, Proquest
search terms: audio, vocal, speech, voice, a/d, d/a, analog-to-digital, digital-to-analog, storage, compression, detection, modem, controller